Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application. By the present amendment, claims 1-3, 11, 19 and 21 have been amended. Claims 1-22 are pending in the application.

Listing of Claims:

Claim 1. (*Currently Amended*) A data signal line driving method for driving a plurality of data signal lines respectively so as to fetch a multiphased video signal via a plurality of video signal lines into the data signal lines,

data signal line groups, each including a predetermined number of adjacent data signal lines sequentially connected to each video signal line, being regarded as a single block, the number of data signal line groups being equal to the number of the video signal lines in each block,

said method comprising ~~the steps of~~:

~~gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line, the predetermined number of adjacent data signal lines being equal to the number of the video signal~~

~~lines, a number of data signal line groups equal to the number of video signal lines being regarded as a single block; and~~

fetching the video signal from the video signal lines into the data signal lines in each block in response to a timing pulse generated by a predetermined number of shift registers provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group, there being performed a first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and there being performed a second driving in which one shift register in the block is driven and all data signal lines in each data signal ine group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines ~~wherein a sampling time of the video signal in each data signal line does not change~~.

Claim 2. (*Currently Amended*) A data signal line driving method for driving a plurality of data signal lines respectively so as to (i) multiphase a video signal having a plurality of color signals and (ii)

fetch the video signal via a plurality of video signal lines into the data signal lines,

each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals,

data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block,

said method comprising ~~the steps of~~:

~~causing a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, to constitute each of the video signal lines;~~

~~gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each divisional video signal line so as to respectively correspond to the color signals, the predetermined number of adjacent data signal lines being equal to the number of the video signal lines, said data signal line group being regarded as a single block; and~~

fetching the video signal from the video signal lines into the data signal lines in each block in response to a timing pulse generated by a predetermined number of shift registers provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group, there being performed a first driving in which all shift registers in the block are driven and individual data signal lines of each data signal ine group in the block are driven simultaneously so as to fetch the video signal from the video signal lines, and there being performed a second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines in to the data signal lines ~~wherein a sampling time of the video signal in each data signal line does not change~~.

Claim 3. (*Currently Amended*) A data signal line driving circuit, which drives a plurality of data signal lines respectively so as to fetch a multiphased video signal via a plurality of video signal lines into the data signal lines, comprising:

data signal line groups, each ~~group comprising~~ including a predetermined number of adjacent data signal lines sequentially connected to each video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block, ~~when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line, the predetermined number of adjacent data signal lines being equal to the number of the video signal lines, a number of data signal line groups equal to the number of video signal lines being regarded as a single block, wherein a sampling time of the video signal in each data signal line does not change~~

the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group,

the video signal fetching section performing:

first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as t fetch the video signal from the video signal lines into the data signal lines; and

second driving in which one shift register in the block is driven an all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines.

Claim 4. (*Previously Presented*) The data signal line driving circuit as set forth in claim 3, wherein the video signal fetching section includes drive switching means for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

Claim 5. (*Previously Presented*) The data signal line driving circuit as set forth in claim 4, wherein:

the video signal fetching section includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and

the drive switching means switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

Claim 6. (*Previously Presented*) The data signal line driving circuit as set forth in claim 5, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching means between the first driving and the second driving.

Claim 7. (*Previously Presented*) The data signal line driving circuit as set forth in claim 3, wherein the video signal fetching section includes a drive switching circuit for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving

in which all the data signal lines of the data signal line groups are driven at the same time.

Claim 8. (*Previously Presented*) The data signal line driving circuit as set forth in claim 7, wherein:

the video signal fetching section includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and

the drive switching circuit switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

Claim 9. (*Previously Presented*) The data signal line driving circuit as set forth in claim 8, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching circuit between the first driving and the second driving.

Claim 10. (*Original*) The data signal line driving circuit as set forth in claim 3, wherein the data signal line groups are data signal line sets each of which is made up of a predetermined number of data signal

lines respectively corresponding to color signals contained in the video signal fetched into the data signal lines.

Claim 11. (*Currently Amended*) A data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (i) multiphase a video signal having a plurality of color signals and (ii) fetch the video signal into the data signal lines,

each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals, said circuit comprising:

data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block; and

~~a plurality of divisional video signal lines, divided so as to correspond to each of the color signals, which constitute each of the video signal lines; and~~

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block, ~~when~~

~~gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines connected to each divisional video signal line, the predetermined number of data signal lines being equal to the number of the video signal lines, said data signal line group being regarded as a single block~~.

the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group,

the video signal fetching section performing

first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and

second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines.

Claim 12. (*Previously Presented*) The data signal line driving circuit as set forth in claim 11, wherein the video signal fetching section includes drive switching means for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

Claim 13. (*Previously Presented*) The data signal line driving circuit as set forth in claim 12, wherein:

the video signal fetching section includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and

the drive switching means switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

Claim 14. (*Previously Presented*) The data signal line driving circuit as set forth in claim 13, wherein the video signal fetching section

includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching means between the first driving and the second driving.

Claim 15. (*Previously Presented*) The data signal line driving circuit as set forth in claim 11, wherein the video signal fetching section includes a drive switching circuit for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

Claim 16. (*Previously Presented*) The data signal line driving circuit as set forth in claim 15, wherein:

the video signal fetching section includes a shift register for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and

the drive switching circuit switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

Claim 17. (*Previously Presented*) The data signal line driving circuit as set forth in claim 16, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching circuit between the first driving and the second driving.

Claim 18. (*Previously Presented*) The data signal line driving circuit as set forth in claim 11, wherein the data signal line groups are data signal line sets each of which is made up of a predetermined number of the data signal lines corresponding to color signals contained in the video signal fetched into the data signal lines, and wherein the number of divisional video signal lines is the same as the number of data signal lines connected to each of the divisional video signal lines.

Claim 19. (*Currently Amended*) A display device, comprising:

a display panel which includes (i) a plurality of data signal lines, (ii) a plurality of scanning signal lines provided so as to cross the data

signal lines, and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines, a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines, said video signal being retained;

a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal; and

a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal, said video signal being multiphased, and being supplied to the data signal lines via a plurality of video signal lines, each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to color signals wherein

the data signal line driving circuit, which drives said plurality of data signal lines respectively so as to fetch the multiphased video signal via said plurality of video signal lines into the data signal lines, includes:

data signal line groups, each ~~group comprising~~ including a predetermined number of adjacent data signal lines for fetching a single

color signal that are sequentially connected to each ~~video signal line~~ divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block, ~~when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each video signal line, the predetermined number of adjacent data signal lines being equal to the number of the video signal lines, a number of data signal line groups equal to the number of video signal lines being regarded as a single block, wherein a sampling time of the video signal in each data signal line does not change.~~

the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group,

the video signal fetching section performing

first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and

second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines.

Claim 20. (*Original*) The display device as set forth in claim 19, wherein the data signal line driving circuit, the scanning signal line driving circuit, and the pixels are formed on the same substrate.

Claim 21. (*Currently Amended*) A display device, comprising:

a display panel which includes (i) a plurality of data signal lines, (ii) a plurality of scanning signal lines provided so as to cross the data signal lines, and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines, a video signal for displaying an image being fetched from the data signal lines into the pixels in

synchronism with a scanning signal supplied from the scanning signal lines, said video signal being retained;

a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal; and

a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal, said video signal being multiphased, and being supplied to the data signal lines via a plurality of video signal lines, wherein

the data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (a) multiphase the video signal having a plurality of color signals and (b) fetch the video signal into the data signal lines, each video signal line including a plurality of video signal lines divided so as to respectively correspond to color signals, comprising ~~includes~~:

~~a plurality of divisional video signal lines, divided so as to respectively correspond to the color signals, which constitute each of the video signal lines; and~~

data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are

sequentially connected to each divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block ~~when gathering data signal line groups, each group comprising a predetermined number of adjacent data signal lines sequentially connected to each divisional video signal line so as to respectively correspond to the color signals, the predetermined number of adjacent data signal lines being equal to the number of the video signal lines, said data signal line group being regarded as a single block, wherein a sampling time of the video signal in each data signal line does not change.~~

the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group,

the video signal fetching section performing

first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and

second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines.

Claim 22. (*Original*) The display device as set forth in claim 21, wherein the data signal line driving circuit, the scanning signal line driving circuit, and the pixels are formed on the same substrate.